REMARKS

This responds to the Office Action mailed on July 11, 2007.

Claims 3-4, 14-15, 19 and 42-43 are amended to independent form including all limitation of the claims from which they depended; as a result, the allowed claims are 5, 9, 16, and 37-40 and the allowable claims are 3-4, 14-15, 19 and 42-44. No new matter is added.

Please charge Deposit account 19-0743 for the seven additional independent claim fees ($1,470.00), and any other required fee.

Claim Rejections Under 35 U.S.C. § 102(e)

1) The Applicable Law for Rejections under 35 U.S.C. § 102

35 U.S.C. 102 Conditions for patentability; novelty and loss of right to patent.

> A person shall be entitled to a patent unless –
> ...
> (e) the invention was described in
> > (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> > (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language;

For a cited reference to be prior art within the meaning of 35 U.S.C. § 102(e), all of the claim limitations must be anticipated by the cited reference. (See MPEP 2131: "**A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.**" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.1987).) MPEP 2131 further details: "The identical invention must be shown **in as complete detail as is contained in the ... claim**." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir.1989.) The elements must be arranged as required by the claim, but this is not an

ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

2) Analysis of the 35 U.S.C. § 102 Rejection of Claims

Claims 1-2, 6-8, 10-13, 17-18, 20-22, 25-27, 30-36 and 41 were rejected under 35 U.S.C. § 102(e) for anticipation by Kolichtchak (US Publication 2003/0014667) – hereinafter, "*Kolichtchak*." Applicant respectfully traverses. The Examiner asserted:

> "Regarding claims 1-2, 10-13, 21-22, 27, 32-35 and 41, Kolichtchak discloses a system comprising a memory (Figure 1, Reference 110); a plurality of pages held in the memory (section 0009); an instruction translation lookaside buffer (ITLB) (Figure 1, Reference 190); a fist data translation lookaside buffer (DTLB) (Figure 1, Reference 180); a translation lookaside buffer [inherent; when a miss occurs in the ITLB, a miss handler [software/code] retrieves the entry from the page table and when a miss occurs in the DTLB a miss handler retrieves the missed page entry from the page table); an executable/non-executable (x) indicator [user/supervisory mode] associated with each page in memory (Figure 2, bit 2; section 0011) wherein the TLB miss handler sets the x-indicator for a particular page to indicate non-executable when that page is accessed in a mode that allows writing to that page, and wherein the ITLB refuses to allow instructions from a page with an associated x-indicator of non-executable to be loaded [section 0014].
>
> Regarding claims 6, 8, 18, and 20, Kolichtchak discloses a write bit associated with each page in memory that indicates the respectiye page is writable (Figure 2, bit 1; section 0011)
>
> Regarding claims 7 and 17, Kolichtchak discloses a page table used to translate a virtual address to a real address, wherein the x-indicator for each page is held in the page table entry associated with that page (Figure 2, bit 2; section 0011).
>
> Regarding claims 25-26, 30-31 and 36, Kolichtchak discloses translating the address for the data access also including setting the non-executable indication for a page holding the data access address on if a write indication is set for that page (Figure 3, Reference 310)."

Please again see Applicant's arguments filed in the Amendment and Response filed November 17, 2006 for Applicant's response to claims 1-2, 6-8, 10-13, 17-18, 20-22, 25-27, 30-36.

The Examiner responded to Applicants arguments regarding claims 3-4, 14-15, and 42-44 by saying the arguments were considered but were moot in view of the new ground(s) of

rejection. However, there were no new grounds of rejection—rather the Examiner indicated claims 3-4, 14-15, 19 and 42-44 were allowable.

The Examiner also responded saying "The Applicant argues that *Kolichtchak's* U/S flag is not an execute/non-execute bit since if the U/S flag is marked supervisor and the processor in supervisor mode, it does not cause the ITLB to refuse to allow instructions to be loaded or executed. The Examiner disagrees, claims are examined given the broadest reasonable interpretation. In this case, Kolichtchak teaches that when a page is non-executable the privilege is set to supervisor mode which prevents execution of the page (loading, etc.) by users having a user privilege only. Hence, *Kolichtchak* refuses access to those pages by users having only a user privilege (refer to section 0011; lines 18-21; section 0014)." The Applicant respectfully submits that the broad interpretation of the Examiner is not reasonable, since *Kolichtchak's* paragraph/section [0011] says

> "The operating system and kernel mode programs operate in the supervisor mode, using memory pages having the supervisor flag set. When the processor is in supervisor mode, it can access all pages; **when in user mode**, it can access only user-level pages. When the processor tries to access a page having its supervisor flag set, a **page fault** occurs."

and then paragraph [0014] says

> "In normal operation, if the same page table entry is cached in both the DTLB and the ITLB, the entries in both TLBs would be identical. The PaX technique, however, forces the DTLB and ITLB into inconsistent states in such a way that only data read/write accesses are allowed and code execution prohibited. More specifically, for those pages desired to be non-executable, the **PaX technique creates PTEs for those pages with the user/supervisor flag U/S set in the supervisor (i.e., "S")** state and generally keeps the PTEs in the S state. The PaX technique next **modifies** the operating system's **page fault handler** in two ways. First, **when the ITLB is filled**, as happens when an instruction is to be executed from a memory page, a page fault is generated, and the modified page fault handler responds by **terminating the program** that attempted the execution. Second, **when the DTLB is filled**, as happens when data is to be accessed (i.e., written or read to/from a memory page), a page fault is also generated, and the modified page fault handler responds by **flushing both TLBs, changing the user/supervisor flag U/S to the user state (i.e., "U"), accessing the page, and changing the user/supervisor flag U/S back to the S state** before resuming operation of the program that attempted the access."

Thus, contrary to the assertion of the Examiner, access to memory is not refused, rather a page fault is generated and the page fault handler flushes both TLBs, sets the U/S bit to USER state, **accesses the page, then sets the U/S bit back to S** (which allows all accesses whether a page is U or S). Thus, the **U/S bit** described in these paragraphs does not refuse to allow instructions from a page that has been accessed in a mode that allows writing to that page, but rather the **page-fault handler** terminates the program that caused a page fault when the ITLB is filled. The termination is not based on the setting of the U/S bit. On the other hand, when the DTLB is filled (due to a **read or write**), the page fault handler again sets the U/S bit to USER, accesses the page, then sets the U/S bit to SUPERVISOR.

This fails to meet any reasonable interpretation of the recitation of claim 1

> an executable/non-executable (x) indicator associated with each page in memory wherein the TLB miss handler sets the x-indicator for a particular page to indicate "non-executable" when that page is accessed in a mode that allows writing to that page, and wherein the ITLB refuses to allow instructions from a page with an associated x-indicator of "non-executable" to be loaded

Further, if one looks to paragraph [0018], one sees that in one respect, the *Kolichtchak* sets the user flag on a page if the page is **non-executable**, and sets a supervisor flag in a page entry table associated with a writable page. (Also paragraph [0027] says "**the method 300 sets** (310) the supervisor flag (i.e., setting the user/supervisor flag U/S to the "S" state) in the PTEs for **all writable pages**", paragraph [0028] says "Broadly speaking, the method 400 detects and possibly suppresses user mode programs that attempt to execute from a writable page. The method 400 detects and interrupts these exceptions and takes alerting and/or avoidance measures when the exception would involve execution from writable memory. For other accesses to a writable page, the method 400 temporarily clears the supervisor flag (i.e., sets the user/supervisor flag U/S to the "U" state) in the associated page table entry in the DTLB for that page, just to allow that access to the page.") Thus, *Kolichtchak* describes ***something in the method*** (there is no description "the **TLB miss handler** sets the x-indicator" as recited in claim 1) setting the S bit, and this is done on all pages that are writable, NOT "**when that page is accessed in a mode that allows writing** to that page. (see also claim 1 of *Kolichtchak:* "A page fault proxy handler for connection to an original page fault handler and a paging table in which **supervisor flags for all entries for all writable memory pages have been pre-**set, the page fault proxy handler

comprising: a page fault detector; a mitigation module; a **page fault filter**, connected to the page fault detector, wherein the filter **passes to the original page fault handler page faults not arising from an attempt to access a writable page by a user mode program**; a controlled memory access module, wherein the controlled memory access module permits a user program to **access a writable page of memory by changing an associated supervisor flag in the paging table**; and an execution address checker, connected to the page fault filter, the mitigation module and the controlled memory access module, wherein the execution address checker passes to the mitigation module only **page faults arising from an attempt by a user mode program to execute from a predetermined section of executable memory**, and wherein the execution address checker passes to the controlled memory access module page faults arising from any other attempt by a user mode program to access a writable page. " The S bit on a page of *Kolichtchak* is analyzed by its page-fault handler, not "wherein the ITLB refuses to allow instructions from a page with an associated x-indicator of 'non-executable' to be loaded".)

Accordingly, the reference fails to describe or suggest all of the elements of the present claims. Reconsideration and an early indication of allowance are respectfully requested.

Please see the MPEP 2106 Requirements in interpreting means-plus-function claims.

In the 8/10/2007 Office Action, the Examiner again failed to provide the required analysis showing equivalent structures, material, or acts described therein (for translating addresses for the data versus translating addresses for instructions) to perform the functions as recited in claim 32. Consequently, the Examiner has failed to set forth a proper *prima facie* case of anticipation under 35 U.S.C. § 112 paragraph 6. Additionally, the claim as previously amended provides further recitation not found in the cited reference. Thus, claim 32 overcame the Examiner's rejection under 35 U.S.C. § 102(e). Reconsideration and an early indication of allowance are respectfully requested.

Claims 33-36 depend from claim 32 and include the recitations of claim 32 by their dependency. Further regarding claim 33-36, please see Applicant's arguments filed November 17, 2006. Reconsideration and an early indication of allowance are respectfully requested.

Allowable Subject Matter

Claims 5, 9, 16, and 37-40 have been allowed.

Claims 3-4, 14-15, 19 and 42-44 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 3-4, 14-15, 19 and 42-43 are rewritten to independent form, and claims 44 has been amended to depend on claim 43. The other claims depended from claims that appear allowable for the reasons recited above. Reconsideration and allowance is respectfully requested.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (952) 435-0201 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this _13th__ day of November 2007.

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